Claims:

1. A circuit assembly for generating pulses sustaining or "plucking" RF oscillations in a resonant circuit of transponder having no battery power supply in which the supply voltage needed for its operation is obtained from a RF carrier oscillation pulse defined in time exciting the resonant circuit into oscillation and used to charge a storage element whose charging voltage forms the supply voltage, in which a sustaining or plucking pulse is generated every time the amplitude of the RF oscillations drops below a defined threshold value and its momentary value is in a defined relationship to a reference voltage changing in time as the charging voltage of a capacitor and wherein a switch is provided which can be switched on for the duration of the plucking pulse for connecting the storage capacitor to the resonant circuit, characterized in that in that a closed control loop (34, 38) is provided which varies the slope of the reference voltage curve between two plucking pulses (PLUCK) in the direction of maintaining the predefined relationship between the momentary value of the RF oscillations (HF1) and the reference voltage (VPEAK).

2. The circuit assembly as set forth in claim 1, characterized in that the closed control loop contains a threshold switch (82) to which the difference between the momentary value of the RF oscillations (HF1) and the reference voltage (VPEAK) is applied and which changes its switching condition and generates an enable signal (PEAK) when the difference attains the predefined relationship, that the closed control loop further contains a counter circuit (38) to which the enable signal (EN-PLUCK) is applied and which as controlled by the clock pulses (HFCLK) derived from the RF oscillations (HF1) increments its count on every clock pulse when no enable signal (PEAK) is present and decrements its count when the enable signal is present, and that a current supplied to the capacitor (70) for generating the charging voltage serving as its reference voltage is varied as a function of each count of the counter circuit (38).

3. The circuit assembly as set forth in claim 2, characterized in that the counter circuit (38) contains an two-stage up/down counter (116, 118) and a logic circuit (110) which prevents a change in the count of the up/down counter (116, 118) on every clock pulse when the highest and lowest count is attained, even in the absence or presence of enable signals (PEAK).